High Speed & Low Power Comparator Designs for Flash ADC

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ABSTRACT*:* In this paper the design of low power arm latch comparator for 4 bit flash ADC was presented. The 4 bit Flash ADC required 15(2^{N-1}) comparators and a thermometer code word to binary code encoder. The major issue in the design of Flash ADC is the large power consumption because of the large number of comparators used in it. So in order to reduce the power consumption of a Flash ADC, we have design a comparator with very low power consumption. Different comparators are designed and their power consumptions are observed. The comparator with lowest power consumption is selected. All comparators are designed and simulated in CMOS 180nm and 45nm technology. The schematic of the all circuits are design with cadence virtuoso.

Index Terms—Cadence virtuoso, CMOStechnology, Flash ADC, latch comparator and low power consumption

I. INTRODUCTION

An Analog to Digital Convertor (ADC) is a device which converts the analog input to the digital output. Among all the ADC's we have Flash ADC is the fastest ADC which samples the given analog voltage in a single clock pulse.

The block diagram of Flash ADC is shown in below figure 1.1. The circuit diagram of N-bit Flash ADC is shown in figure 1.2 which as 2N-1 comparators arranged in sequentially.

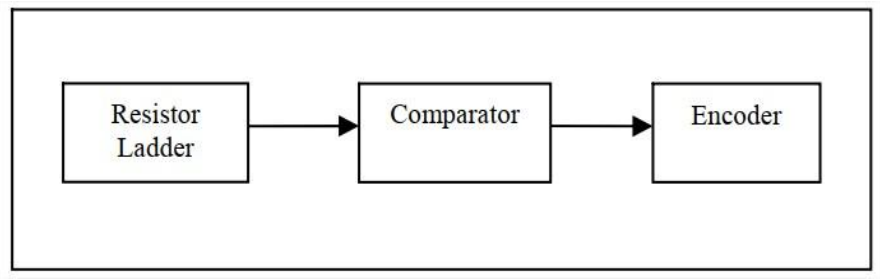

Fig. 1.1 General Block Diagram of ADC

A comparator design is more important when you design flash ADC. Because it consumes more power in the whole design and there are 2N-1 comparators which consumes lot of power [1]. In the Section II we proposed different types of comparator designs. The one which consumes low power is selected for ADC design.

The comparator is also called as 1-bit ADC and it is one of the most important block in ADCs. The basic configuration of the comparator can be one of the three types, namely (i) Simple inverter, (ii) Operational amplifier (in open loop configuration), and (iii) Differential amplifier along with cross – coupled latch. Op-amp is the most widely used component in

electronics and normally usedwith negative feedback. It can also be used as comparator in open loop configuration.

In the analog-to-digital conversion, the input is sampled in first step and applied to the combination of comparator to determine the digital output of analog input.

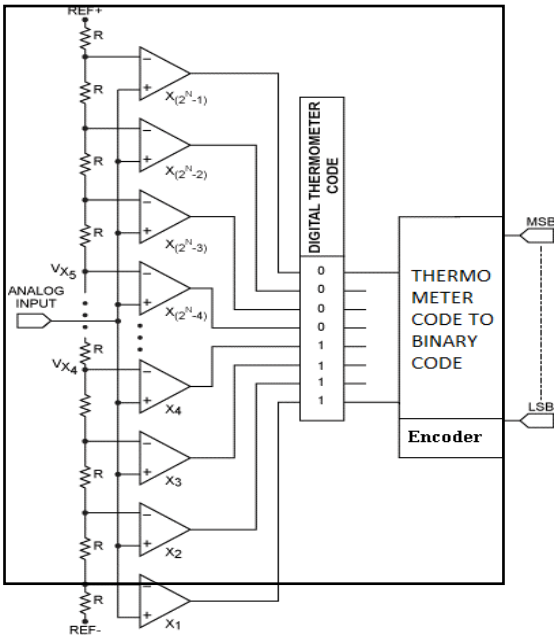

Fig. 1.2 N-Bit Flash ADC

The conversion speed of these comparators is restricted by the decision making responsetime of it. The basic application of a CMOS comparator is to find out whether a given signal is greater or smaller than the reference signal. The schematic symbol of a comparator is depicted in Fig. 1.3.

The comparator can be thought of as a decision-making circuit. If VINP (V+ or VP) input of the comparator is at a greater potential than VINN (V- or Vn) input, the output of the comparator is at Vdd (High or Logic 1), whereas if VINP input is at a potential less than VINN input, output of the comparator is at Vss (Low or Logic 0).

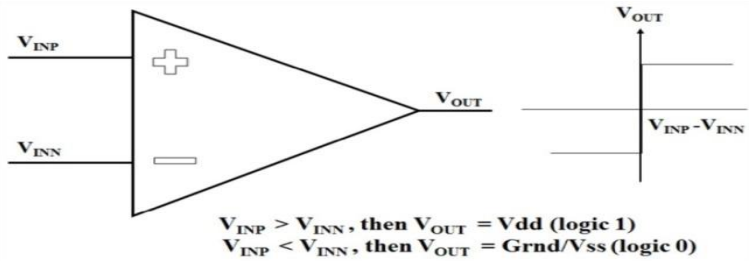

Fig.1.3. Schematic of Comparator

II. COMPARATOR

A. Conventional Dynamic Comparator

Comparator is the major block of the Flash ADC. Inputs are connected to the inverter and non-inverting terminals will gives the output either logic high or low. In this design, the

input is given to the non inverting terminal of the comparator and reference voltage is given to the inverting terminal of the comparator. There are different types of comparator designs. In this paper we have define three designs. Below figure shows the conventional comparator design.

The design is having clocked regenerative latch formed with the two inverters connected cross-coupled manner from M1 to M4.

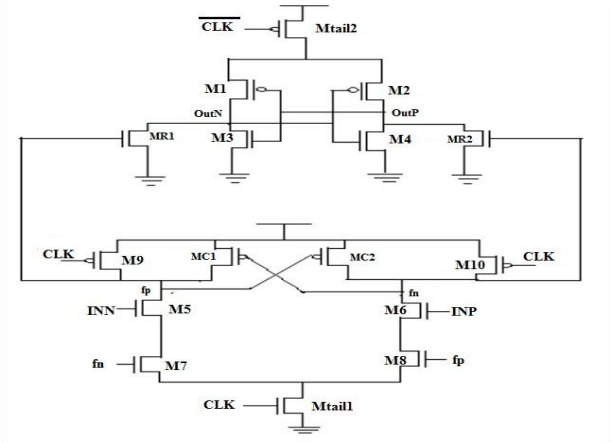

Fig. 2.1 Design of Conventional Dynamic Comparator

Comparator is operated in two different phases that are reset and decision phases. Within the reset phase the clock is low. The tail transistors M1 and Mtail2 are off and transistors M9 and M10 are on this might charge the nodes fp and fn to VDD. The transistors MR1 and MR2 are on when fp and fn attend vdd. The voltage at OutN and OutP nodes discharges through MR1 and MR2 transistors. Within the choice, the phase clock goes to high. The transistors Mtail1 and Mtail2 are ON and M9 and M10 are OFF. During reset phase nodes fp and fn are charged to VDD the transistors M7 and M8 are ON.

Lets consider INP is greater than INN. Within the reset phase, the nodes fp and fn are charged to VDD. Since INP is greater the node fn is discharging fastly compared to fp node. When fn goes to ground level the transistor MC1 will get ON. This makes the node fp to agitate to VDD. When fp charges to VDD the transistor MC2 will pack up this makes the node fn to discharges completely. Since fp is charged to VDD this might makes the transistor MR1 activate. The node OutN will discharges and which is connected to latch will make the OutP is charged to high.

B. Strong ARM Latch Comparator

Strong ARM Latch Comparator is used for medium frequency applications. It consumes zero static power and directly produces rail to rail output it means, whose dynamic range is able to reach the extremes of the supply voltage [3]. Figure 2.2 shows the Strong ARM Latch Comparator.

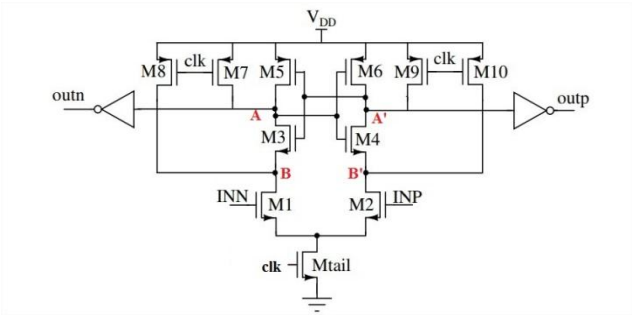

Fig. 2.2 Strong ARM Latch Dynamic Comparator

When the clock is low the transistors M5 to M10 are ON because of PMOStransistors. Theinternal capacitors at Nodes A, A' and B, B' are charge to VDD. The outn and outp are at zero state because its connected to inverters. When the clock goes high comparator will be activated and Mtail transistor is on.

Let INP is greater than INN, the transistor M2 is on faster than the M1 and it discharges quickly through Mtail transistor. Once the potential at B' goes to ground and it is connected to invertor circuit the outP becomes high. Since the latch is connected in above i.e cross coupled of invertors the outN becomes low when A' becomes low. (A' = B')

One of the restrictions during this topology is that the clock feedthrough problem. The voltages at A and A' follow the clock for a small period, leading to spike >VDD when the clock goes High, and another spike

C. Modified Strong ARM Latch Dynamic Comparator

The below Figure 2.3 shows Modified Strong ARM Latch Comparator reduced transistor count from the original. Here the Inverting and Non-inverting transistors are placed in between latch.

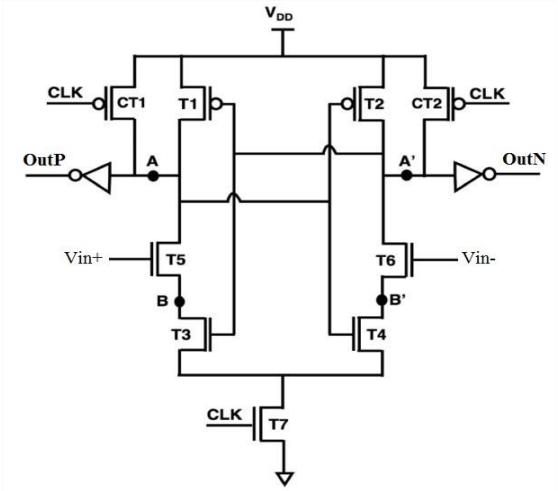

Fig. 2.3 Modified Strong ARM Latch Dynamic Comparator

When clock goes low the transistors CT1 and CT2 are on. The nodes A and A' are charged to VDD. When clock goes high transistor T7 is on and comparator is on. When Vin- is greater than Vin+ , the charge at node A' discharges quickly compared to charge at A. When charge at A' goes to ground level the OutN becomes High.

Since, the comparator is designed for Flash ADC and it requires only one outputto compareboth non-inverting and inverting signals.

Hence, Fig. 2.3 can be modified as Fig. 2.4 so that the transistor count can be reduced. The transistor CT2 and invertor at outN are removed.

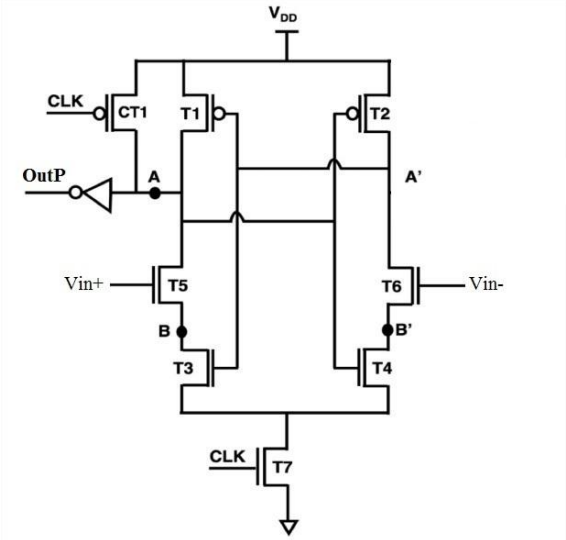

Fig. 2.4. Modified Strong ARM Latch Dynamic Comparator

III. RESULTS AND COMPARISION

All the comparators are designed and simulated in cadence virtuoso 180nm and 45nm technologies.

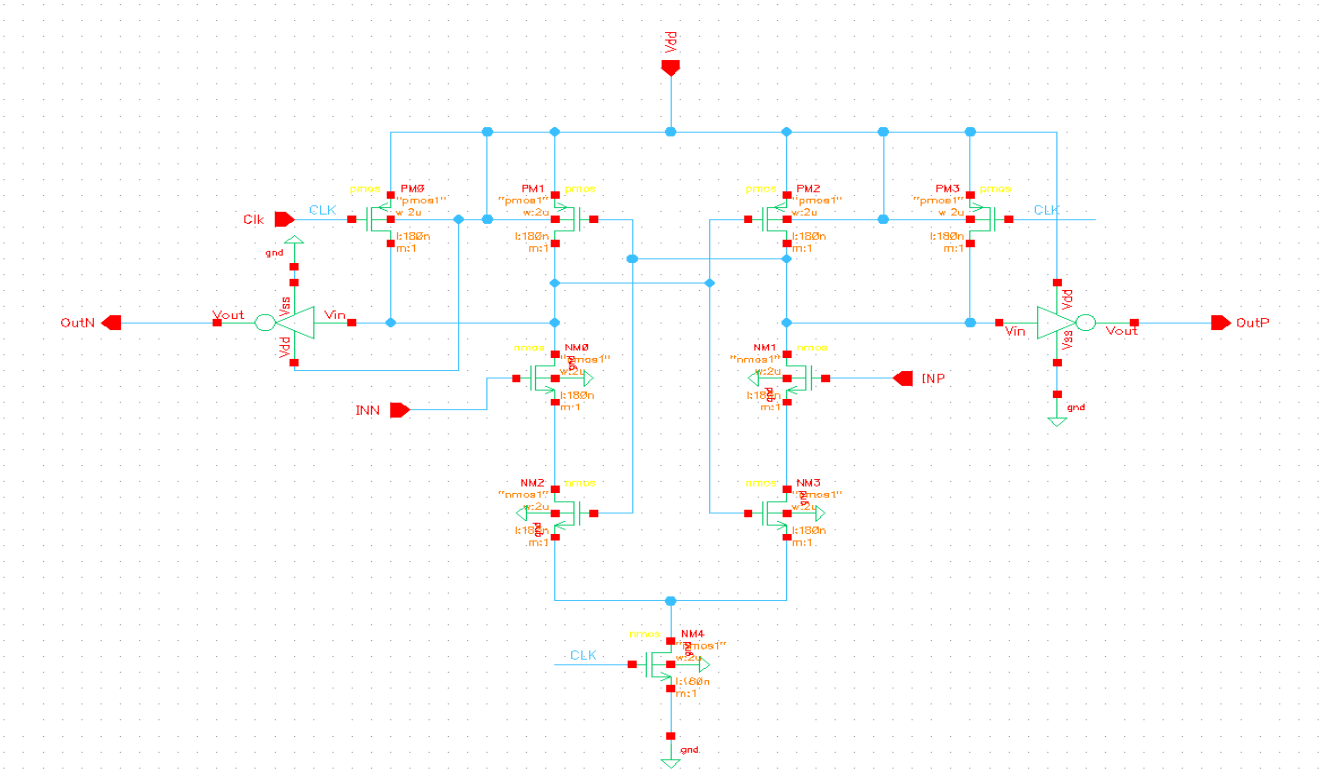

Fig. 3.1. Schematic Design of Modified Strong ARM Latch Dynamic Comparator in cadence virtuoso

Fig. 3.2 shows the results of comparator when sinusoidal signal (2V p-p and) is given to non-inverting terminal and constant dc signal is given to inverting terminal of a comparator.

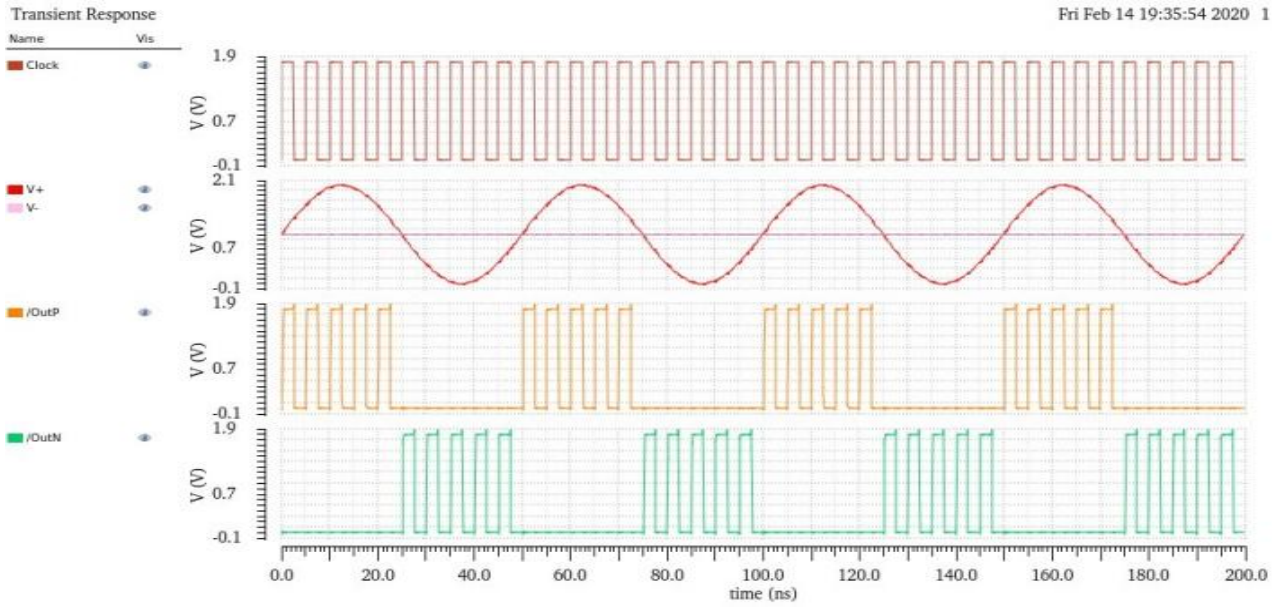

Fig. 3.2 Results of a Comparator

Tables I&II show the comparison results of all the designs and input values for the comparator.

Table I. Comparison Results of Comparator

	180nm		45nm	
Comparator	Power (μW)	Delay (ns)	Power (μW)	Delay (ns)
Conventional Dynamic Comparator	54.735	26.72	0.642	28.53
Strong Arm Latch Comparator (15T)	39.97	25.56	0.308	26.57
Modified Strong Arm Latch Comparator (13T)	32.50	25.53	0.242	26.54

Table II. Input Values for Comparator

	180nm	45nm
VDD	2V p-p	1V p-p
Input Freq.	20Mhz	20Mhz
Sampling Freq.	200Mhz	200Mhz

IV. CONCLUSION

All the designed comparators are simulated in 180nm and 45nm using Cadence Virtuoso. The power of Modified Strong ARM Latch Dynamic Comparator reduced 40.6% and 18.68% compared Conventional Dynamic Comparator and Strong Arm Latch Comparator.

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